CLAIMS

What is claimed is:

1. A method comprising:

receiving input data;

scrambling the input data;

modulating the scrambled input data;

spreading the modulated scrambled input data with a Walsh code to create Walsh chips; and

spreading each Walsh chip with a pseudonoise (PN) sequence creating an output signal.

2. The method of claim 1 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

3. The method of claim 2 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

4. The method according to claim 1, wherein the output signal is communicated to a receiver.

5. The method of claim 4 further comprising the transfer of a payment before the output signal is communicated.

6. The method according to claim 1, wherein the output signal is received by a receiver.

7. A processing system comprising a processor, which when executing a set of instructions performs the method of claim 1.

8. A machine-readable medium having stored thereon instructions, which when executed performs the method of claim 1.

9. An apparatus comprising:

means for receiving input data;

means for scrambling the input data;

means for modulating the scrambled input data;

means for spreading the modulated scrambled input data with a Walsh code to create Walsh chips; and

means for spreading each Walsh chip with a pseudonoise (PN) sequence creating an output signal.

10. The apparatus of claim 9 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

11. The apparatus of claim 10 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

12. The apparatus of claim 9 implemented by an integrated circuit (IC).

13. A machine-readable medium having stored thereon information representing the apparatus of claim 9.

14. An apparatus for creating a signal, comprising:

an input coupled to receive data;

a scrambler having an input and an output, the input coupled to receive the data;

a modulator having an input and an output, the input coupled to receive the scrambler output;

a first spreader having a first input, a second input, and an output, the first input coupled to receive the modulator output, and the second input coupled to receive a Walsh code;

a second spreader having a first input, a second input, and an output, the first input coupled to receive the first spreader output, the second input coupled to receive a PN sequence, and the output being the signal.

15. The apparatus of claim 14 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

16. The apparatus of claim 15 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

17. A system comprising a processor, which when executing a set of instructions, performs the following:

receives input data;

scrambles the input data;

modulates the scrambled input data;

spreads the modulated scrambled input data with a Walsh code to create Walsh chips; and

spreads each Walsh chip with a pseudonoise (PN) sequence creating an output signal.

18. The system of claim 17 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

19. The system of claim 18 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

20. A method for acquiring frequency and timing synchronization in a communication system comprising:

(a) receiving a transmitted signal;

(b) processing the received signal to reduce the frequency offset of the received signal based upon a frequency offset estimate;

(c) despreading the processed received signal with a first despreading sequence to create a first despread signal;

(d) despreading the first despread signal with a second despreading sequence to create a second despread signal;

(e) estimating the frequency offset of the second despread signal to create a frequency offset estimate;

(f) despreading the second despread signal at a first time offset to create a third despread signal;

(g) despreading the second despread signal at a second time offset to create a fourth despread signal; and

(h) comparing the energy of the third and fourth despread signals to determine a second despreading sequence.

21. The method of claim 20 wherein the first despreading sequence is a pseudonoise (PN) sequence.

22. The method of claim 20 wherein the second despreading sequence is a Walsh code of length N.

23. The method of claim 22 wherein the Walsh code index is 2^N-1.

24. The method of claim 20 wherein the second despreading sequence is determined to be one of a plurality of time shifted sequences.

25. The method of claim 20 wherein (b) through (h) are repeated.

26. The method of claim 25 wherein the length of the second despreading sequence is increased for each repetition.

27. The method of claim 26 wherein the final repetition is that in which the sequence length reaches the length of the second spreading sequence that was used to construct the transmitted signal.

28. The method of claim 25 wherein the received signal (b) is the same received signal for each repetition.

29. The method of claim 25 wherein the received signal (b) is a newly received signal for each repetition.

30. A method comprising:

(a) acquiring chip synchronization to a signal spread with a code sequence of length K, where $K=2^m$;

(b) setting an initial detection period of $x=x_0$ chips;

(c) detecting a partial code symbol of length x chips; and

(d) if x=K, declaring symbol synchronization, else setting x=x*2 and repeating (c) and (d).

31. The method of claim 30 wherein the code sequence is a Walsh code.

32. The method of claim 31 wherein the Walsh code has an index of K-1

33. The method of claim 30 wherein the detecting is a plurality of correlations between a received signal and time-shifted versions of the code sequence.

34. The method of claim 33 further comprising choosing the time-shifted code sequence resulting in the highest correlation.

35. The method of claim 30 wherein each chip of the signal is further spread by a pseudonoise code sequence.

36. The method of claim 33 wherein chip synchronization is accomplished by correlating the received signal with a plurality of time-shifted versions of a pseudonoise code sequence.

37. A method for symbol synchronization in a receiver, the method comprising:

(a) receiving a data sequence signal transmitted at a transmit frequency and having scrambling, modulating, Walsh length = N spreading, and PN sequence length = M spreading;

(b) combining the received data signal with a local oscillator (LO) operating at a frequency;

(c) correlating the received data sequence with a locally stored replica of the transmit PN sequence (of length M) to acquire an initial PN sequence alignment with the received data sequence at a PN sequence timing rate;

(d) estimating a frequency offset between the transmit frequency and the local oscillator frequency, based on a phase difference between the first half of the PN sequence correlation and the second half of the PN sequence correlation and adjusting the local oscillator frequency to make the offset smaller;

(e) setting a variable X=1;

(f) correlating a newly received data sequence with the PN sequence and a Walsh code of length 2^X;

(g) picking the highest correlation energy in (f) as a new Walsh boundary;

(h) despreading the newly received data sequence with the Walsh code of length 2^X using the PN sequence timing rate over the new Walsh boundary;

(i) estimating a new frequency offset based on a phase difference between the first half of a PN-Walsh sequence correlation and a second half of the PN-Walsh sequence correlation over a length of $M*2^X$ and adjusting the local oscillator frequency to make the offset smaller;

(j) determining if $2^X=N$ and if so outputting a signal indicating symbol synchronization in the receiver, else setting X=X+1 and going to (f).

38. The method of claim 37 wherein the Walsh code is a Walsh code index 2^N-1.

39. The method of claim 37 wherein a data sequence (a) and a newly received data sequence (f) are the same.

40. An iterative sequential method for frequency and timing synchronization of a scrambled, modulated, Walsh length = N spread, and PN sequence length = M spread transmitted signal, said signal received in a receiver, the method comprising:

(a) acquiring an initial PN synchronization of the received signal based substantially on a locally stored copy of the PN sequence at the receiver;

(b) calculating a frequency offset between the transmitted signal frequency and a local oscillator frequency by calculating a phase estimate between a signal $X_0(t)$ and $X_1(t)$ where:

$$X_0(t) = \sum_{i=0}^{k-1} \left(PN_{i\%M} * W_{\lfloor i/M \rfloor} * r_{i+t} \right)$$

$$X_1(t) = \sum_{i=k}^{2k-1} \left(PN_{i\%M} * W_{\lfloor i/M \rfloor} * r_{i+t} \right)$$

and,

k=M/2, M, 2M, ..., (N/2)M

(c) adjusting the local oscillator frequency to provide lower offset

(d) despreading the received data signal;

(e) calculating two decision metrics Z_0 and Z_1, where:

$$Y(t) = X_0(t) + X_1(t)$$

$$Z_0 = \sum_{r=0}^{R-1} \left(Y[2k*(2r)] - Y[2k*(2r+1)]\right)^2$$

$$Z_1 = \sum_{r=0}^{R-1} \left(Y[2k*(2r+1)] - Y[2k*(2r+2)]\right)^2$$

(f) choosing the higher of Z_0 or Z_1 to determine a symbol synchronization; and

(g) repeating (b) through (f) for k=M/2, M, 2M, ..., (N/2)M.

41. A processing system comprising a processor, which when executing a set of instructions performs the method of claim 40.

42. A machine-readable medium having stored thereon instructions, which when executed performs the method of claim 40.

43. An apparatus comprising:

an input coupled to receive a signal;

a first multiplier having a first input, a second input, and an output, the first input coupled to receive the signal;

a second multiplier having a first input, a second input, and an output, the first input coupled to receive the first multiplier output, the second input coupled to receive a PN sequence;

a third multiplier having a first input, a second input, and an output, the first input coupled to receive the second multiplier output,

a first accumulator having an input and an output, the input coupled to receive the third multiplier output;

a frequency offset estimator having an input and an output, the input coupled to receive the first accumulator output;

a frequency generator having an input and an output, the input coupled to receive the frequency offset estimator output, the output coupled to the first multiplier second input;

a second accumulator having an input and an output, the input coupled to receive the first accumulator output;

a Z-transform block having an input and an output, the input coupled to receive the second accumulator output;

an adder having a positive input, a negative input, and an output, the negative input coupled to receive the Z-transform block output, the positive input coupled to receive the second accumulator output;

a power computation block having an input and an output, the input coupled to receive the adder output;

a third accumulator having an input and an output, and the input coupled to receive the power computation output;

a fourth accumulator having an input and an output, and the input coupled to receive the power computation output;

a threshold block having a first input, a second input, and an output, the first input coupled to receive the third accumulator output, the second input coupled to receive the

fourth accumulator output;

a symbol timing adjustment block having an input and an output, the input coupled to receive the threshold block output;

a Walsh sequence code generator having an input and an output, the input coupled to receive the output of the symbol timing generator, the output coupled to the second input of the third multiplier; and

a symbol detector output signal coupled to receive the first accumulator output.

44. The apparatus of claim 43 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

45. The apparatus of claim 44 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

46. An apparatus comprising:

means for receiving a signal;

means for multiplying the signal and a substantially sinusoidal signal at a frequency;

means for despreading the signal with a PN sequence creating a PN-despread signal;

means for despreading the PN-despread signal with a Walsh sequence creating a PW-output;

means for accumulating the PW-output creating Walsh chip sums;

means for frequency offset estimation;

means for generating the frequency;

means for accumulating the Walsh chip sums;

means for performing a Z transform;

means for computing power;

means for accumulating alternating Walsh chip sums;

means for threshold comparison; and

means for adjusting Walsh symbol timing.

47. The apparatus of claim 46 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

48. The apparatus of claim 34 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

49. The apparatus of claim 46 implemented by an integrated circuit (IC).

50. A machine-readable medium having stored thereon information representing the apparatus of claim 46.

51. A system comprising a processor, which when executing a set of instructions, performs the following:

receives a signal;

multiplies the signal and a substantially sinusoidal signal at a frequency;

despreads the signal with a PN sequence creating a PN-despread signal;

despreads the PN-despread signal with a Walsh sequence creating a PW-output;

accumulates the PW-output creating Walsh chip sums;

estimates frequency offset;

generates the frequency;

accumulates the Walsh chip sums;

performs a Z transform;

computes power;

accumulates alternating Walsh chip sums;

performs threshold comparison; and

adjusts Walsh symbol timing.

52. The system of claim 51 wherein the Walsh code is 2^N-1 where N is the bit length of the Walsh code.

53. The system of claim 51 wherein the PN sequence is of length M and a modulation symbol has a length of N*M chips.

54. A method comprising:

receiving input data to be transmitted;

scrambling the input data;

modulating the scrambled input data;

spreading the modulated scrambled input data with a Walsh code 2^N-1, where N is

the bit length of the Walsh code, to create Walsh chips; and

spreading each Walsh chip with a pseudonoise (PN) sequence, of length M, creating an output data sequence signal;

transmitting at a transmit frequency the output data sequence signal to a receiver;

(a) receiving the data sequence signal transmitted at the transmit frequency;

(b) combining the received data signal with a local oscillator (LO) operating at a frequency;

(c) correlating the received data sequence with a locally stored replica of the transmit PN sequence (of length M) to acquire an initial PN sequence alignment with the received data sequence at a PN sequence timing rate;

(d) estimating a frequency offset between the transmit frequency and the local oscillator frequency, based on a phase difference between the first half of the PN sequence correlation and the second half of the PN sequence correlation and adjusting the local oscillator frequency to make the offset smaller;

(e) setting a variable X=1;

(f) correlating a newly received data sequence with the PN sequence and a Walsh code of length 2^X;

(g) picking the highest correlation energy in (f) as a new Walsh boundary;

(h) despreading the newly received data sequence with the Walsh code of length 2^X using the PN sequence timing rate over the new Walsh boundary;

(i) estimating a new frequency offset based on a phase difference between the first half of a PN-Walsh sequence correlation and a second half of the PN-Walsh sequence correlation over a length of $M*2^X$ and adjusting the local oscillator frequency to make the

offset smaller;

(j) determining if 2^X=N and if so outputting a signal indicating symbol synchronization in the receiver, else setting X=X+1 and going to (f).

55. The method of claim 54 wherein the data sequence (a) and a newly received data sequence (f) are the same.